
# Technical Note

*Accessing BLSPs on Inforce products Powered by Qualcomm® Snapdragon™ 805 Processor (APQ8084 SoC)*

## *BAM Low Speed Peripheral (BLSP) interface ports*

Qualcomm provides access to low speed peripherals that are available on the Snapdragon processors through BLSPs. The ***Bus Access Manager/Module*** (BAM) can be considered as a distributed ***data mover*** (DM). BLSP is a new design on target chipsets that replaces the legacy GSBI core and are implemented within the peripheral subsystem of the Snapdragon 805 processor.

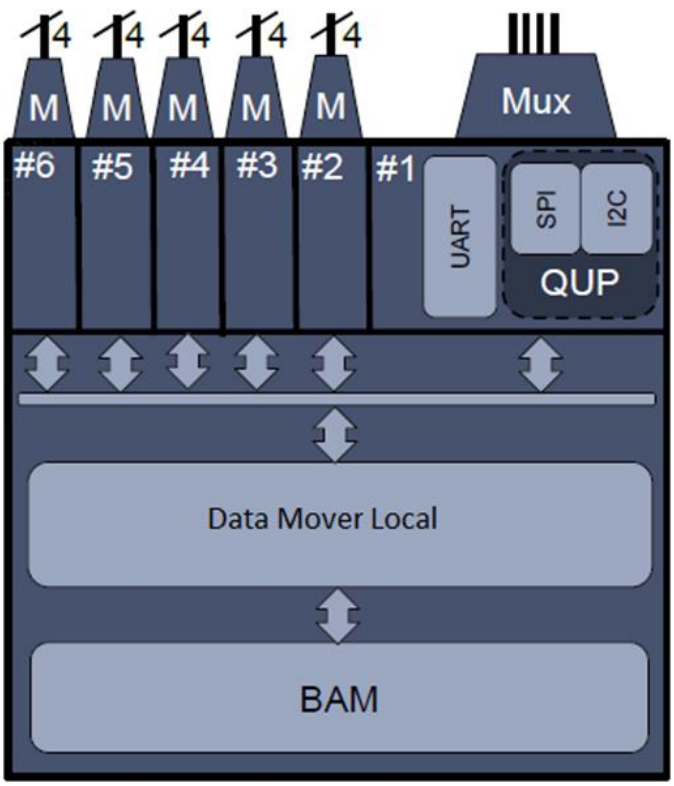


**Figure 1: BL SP interface in the Snapdragon 805 processor**

Target chipsets have one or two BLSP blocks, and each block includes a maximum of six Qualcomm ***Universal Peripheral*** (QUP) and six UART cores. The Qualcomm Universal Peripheral serial engine provides a common datapath that supports multiple mini cores such as I2C , SPI etc. BAM is used to move data to/from the peripheral buffers. Each BLSP peripheral is statically connected to a pair of BAM pipes. BLSP supports both BAM and non-BAM-based data transfers.

## *Supported Protocols*

The supported protocols are

- UART_DM - The UART core can be configured as either an UART, or IrDA interface peripheral. It Utilizes BAM instead of DM to transfer data between its Rx/Tx buffers and system memory
  - ⇒ UART with data rates up to 4 Mbps
    - ◊ Use cases could be serial console for debug and diagnostics, and BT communication
  - ⇒ IrDA
- QUP - Provides a general-purpose data path that supports multiple mini-cores. Each QUP core has a SPI mini-core and an I2C mini-core. Note that only one mini-core can be enabled at a time per QUP core.
  - ⇒ Inter-Integrated Circuit (I2C) with data rates up to 1 Mbps
    - ◊ Use cases could be touchscreen interface, sensors, LED flash
  - ⇒ Serial Peripheral Interface Bus (SPI) with data rates up to 50 Mbps
    - ◊ Use cases could be sensors such as a Gyroscope, accelerometer, magnetometer or a barometer

On the Snapdragon 805 (APQ8084) processor, there are 12 BLSPs that can be configured independently. As a result, a maximum of 12 concurrent BLSPs for any function per port is supported. Internally there are two BLSP wrappers and each BLSP has two sets of six cores—the first set is six UART_DM cores and the other set is six QUP cores. In summary, there are 12 UART_DM cores and 12 QUP cores. A QUP core consists of SPI and I2C. UART_DM will also be multiplexed with User Identity Module (UIM) controllers. BLSPs that can be configured are typically made available on the expansion header of Inforce platforms. Inforce Platform specific details of BLSPs are provided in the following tables.

| BLSP QUP Core | BUS interface |
|---|---|
| BLSP3_0 | SPI |
| BLSP3_1 | |
| BLSP3_2 | |
| BLSP3_3 | |
| BLSP8_0 | UART |
| BLSP8_1 | |
| BLSP8_2 | I2C (used for sensors - LSM330 and thus not available to the user) |
| BLSP8_3 | |
| BLSP10_0 | I2C (used for display touch and thus not available to the user) |
| BLSP10_1 | |

***Table-1:*** On the Inforce 6501 Micro SOM, BLSP3 (4 lines), BLSP10 (2 lines) and BLSP8 (4 lines) are brought out of the B2B connectors. The GPIO mapping and their usage is listed in the above table.

| BLSP QUP Core | BUS interface |
|---|---|
| BLSP2_0 | SPI/UART/I2C |
| BLSP2_1 | |
| BLSP2_2 | |
| BLSP2_3 | |
| BLSP8_0 | I2C |
| BLSP8_1 | |
| BLSP9_0 | SPI/UART/I2C |
| BLSP9_1 | |
| BLSP9_2 | |
| BLSP9_3 | |
| BLSP12_0 | SPI/UART/I2C |
| BLSP12_1 | |
| BLSP12_2 | |
| BLSP12_3 | |

***Table-2:*** On the Inforce 6540 SBC, BLSP2 (4 lines), BLSP8 (2 lines) and BLSP12 (4 lines) are made available on the expansion header. The GPIO mapping and their usage is listed in the table above.

### *Additional information*

To learn more about the processing power, performance, and connectivity options provided by the Snapdragon 805 processor based Inforce 6501 Micro SOM and the Inforce 6540 SBC, please visit www.inforcecomputing.com



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